M-15206 US

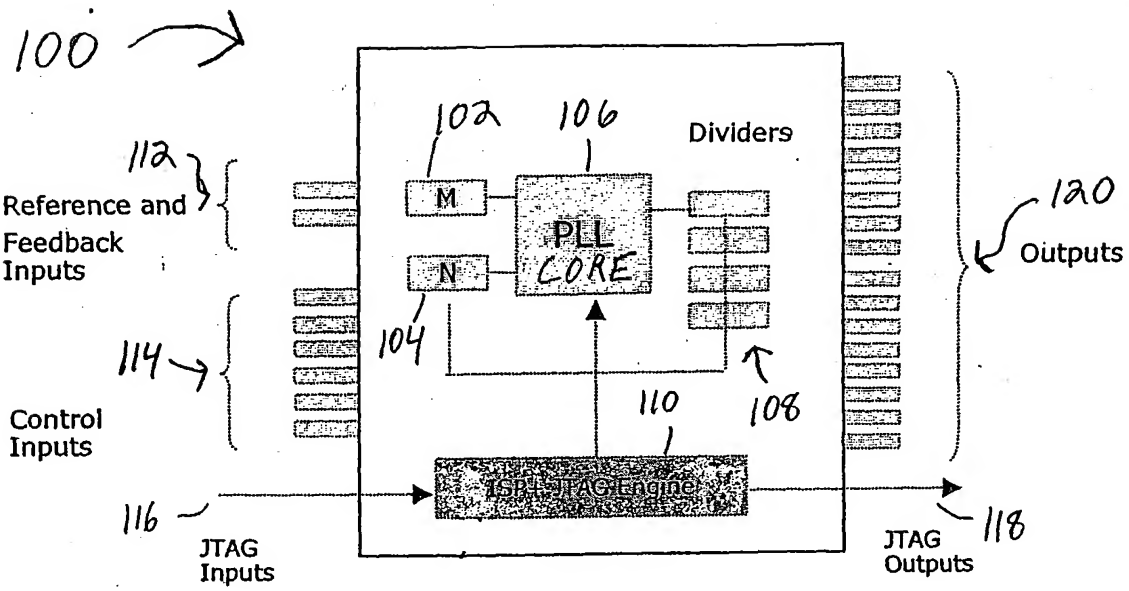


Fig. 1

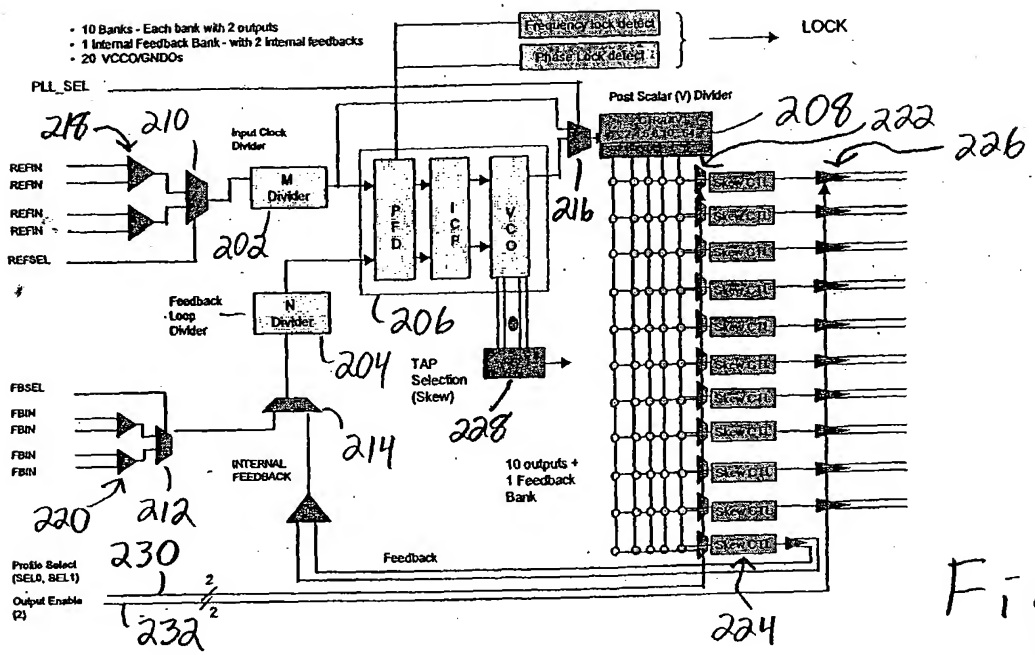


Fig. 2

External Frequ ncy Select Control & Five Diff r nt Frequency Generations

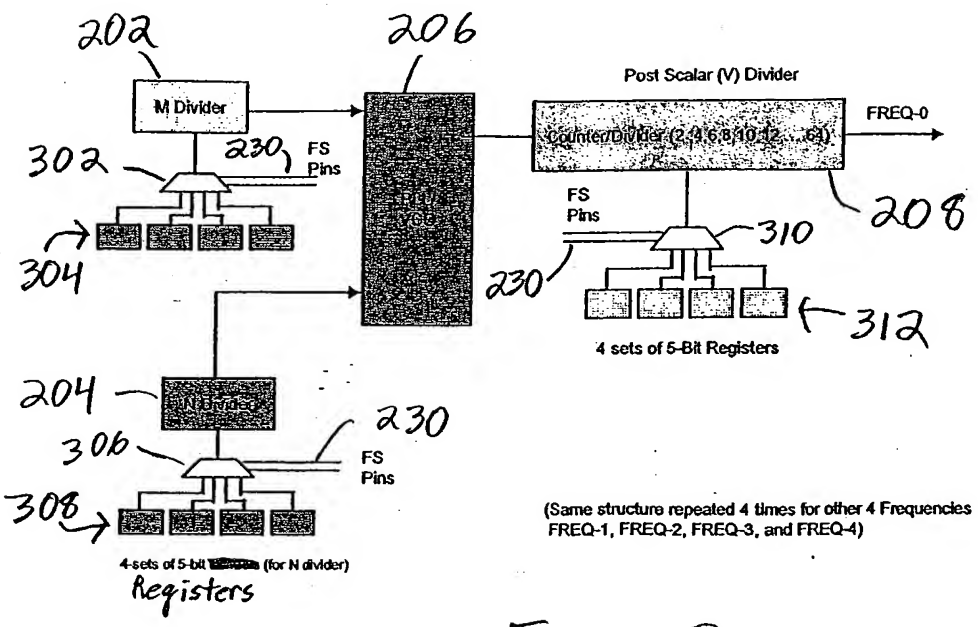


Fig. 3

External Frequency Select Control & Five Different Frequency Generations

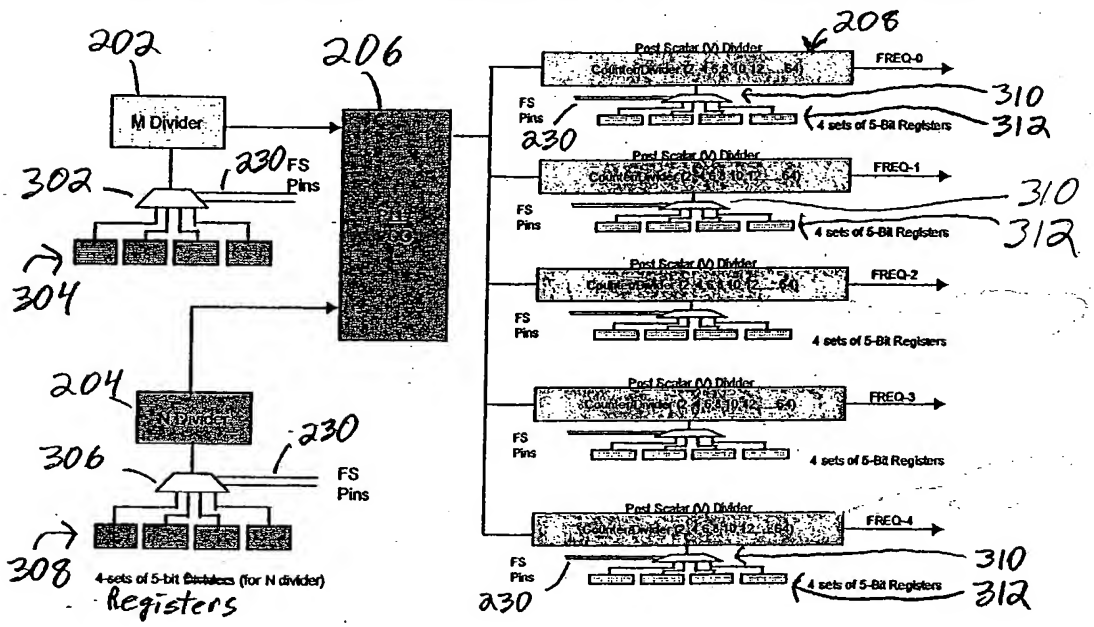


Fig. 4

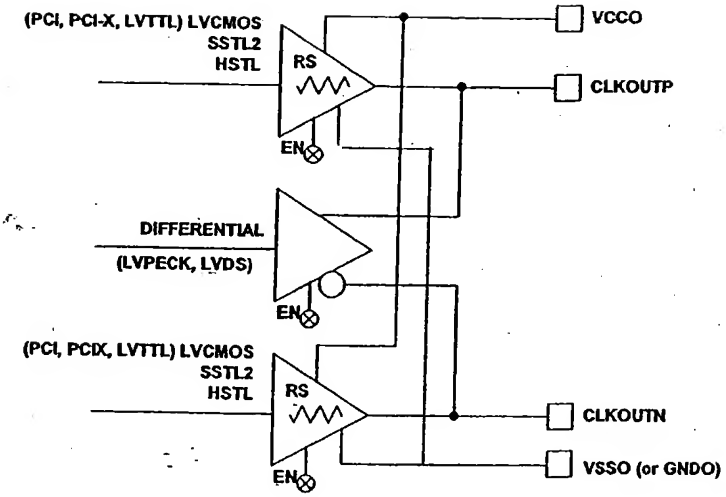

(PCI, PCI-X, LVTTL) LVCMOS
SSTL2
HSTL
RS
EN
VCCO
CLKOUTP
DIFFERENTIAL
(LVPECK, LVDS)
EN
(PCI, PCIX, LVTTL) LVCMOS
SSTL2
HSTL
RS
EN
CLKOUTN
VSSO (or GNDO)

Fig. 5

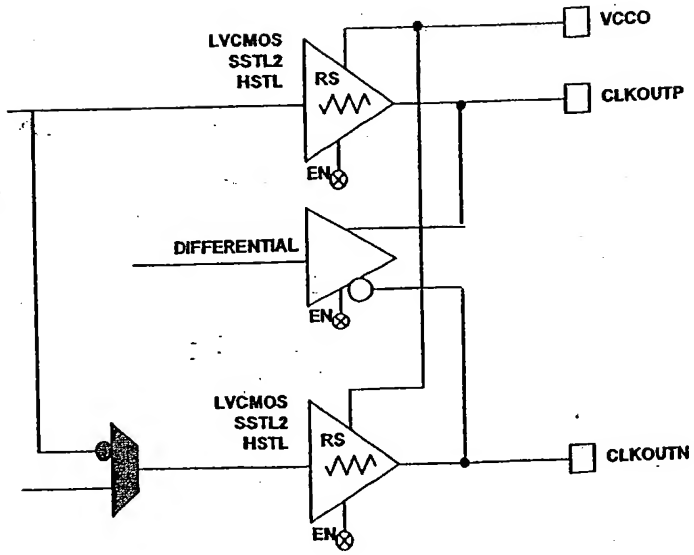

LVCMOS
SSTL2
HSTL
RS
EN
VCCO
CLKOUTP
DIFFERENTIAL
EN
LVCMOS
SSTL2
HSTL
RS
EN
CLKOUTN

Fig. 6

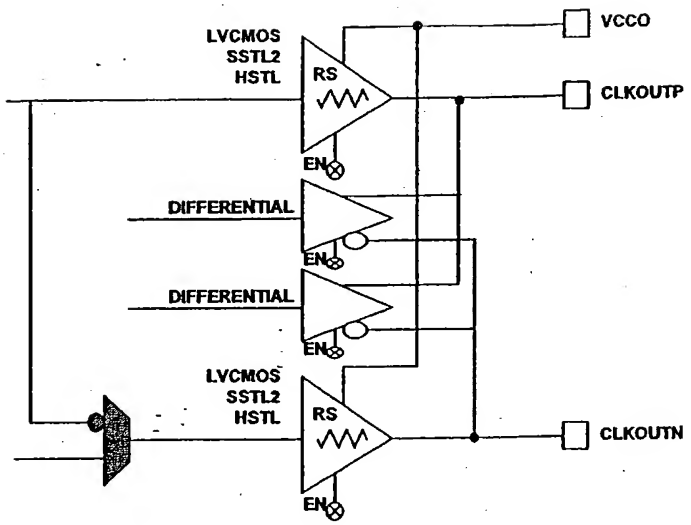
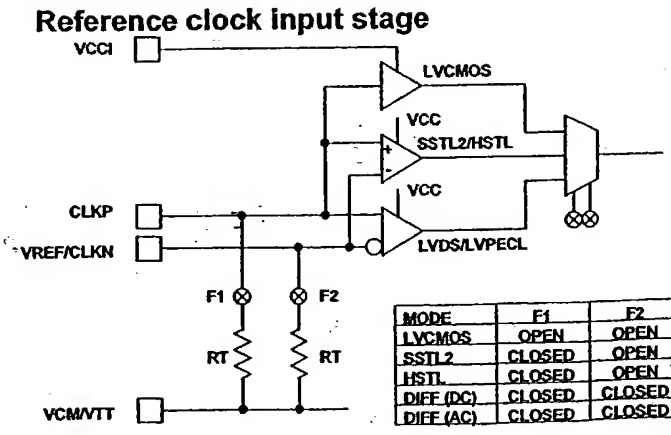


Fig. 7



800

MODE	F1	F2	VREF/CLKN	VCM/VTT
LVCMOS	OPEN	OPEN	NC	NC
SSTL2	CLOSED	OPEN	1.25V	VTT(1.25V)
HSTL	CLOSED	OPEN	0.75V	VTT(0.75V)
DIFF (DC)	CLOSED	CLOSED	CLKN	OPTIONAL
DIFF (AC)	CLOSED	CLOSED	CLKN	VCM

Fig. 8

SSTL2/HSTL input application

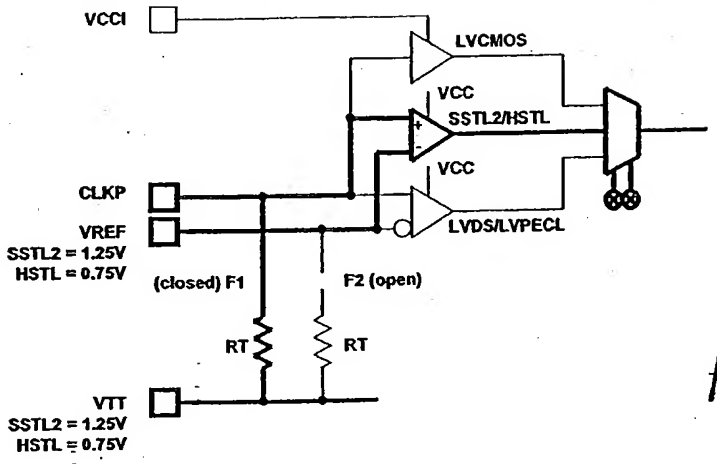


Fig. 9

Alternative DC coupled differential application

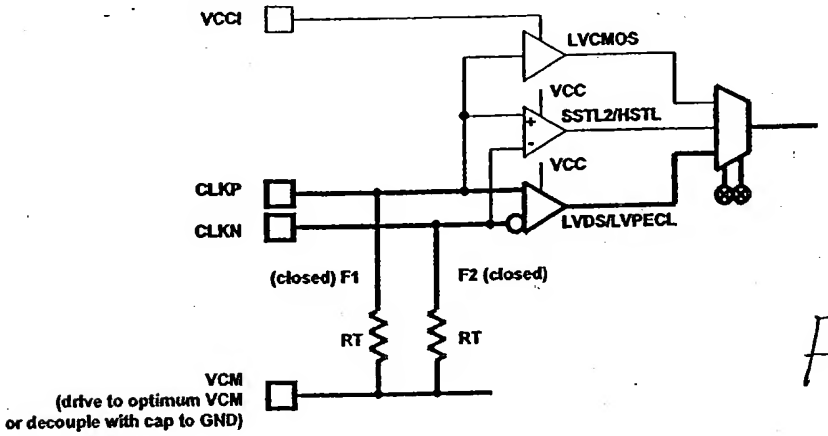
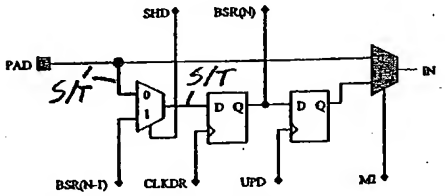


Fig. 10



EXTEST - CDR

Input Boundary Scan Cell

1100

Fig. 11

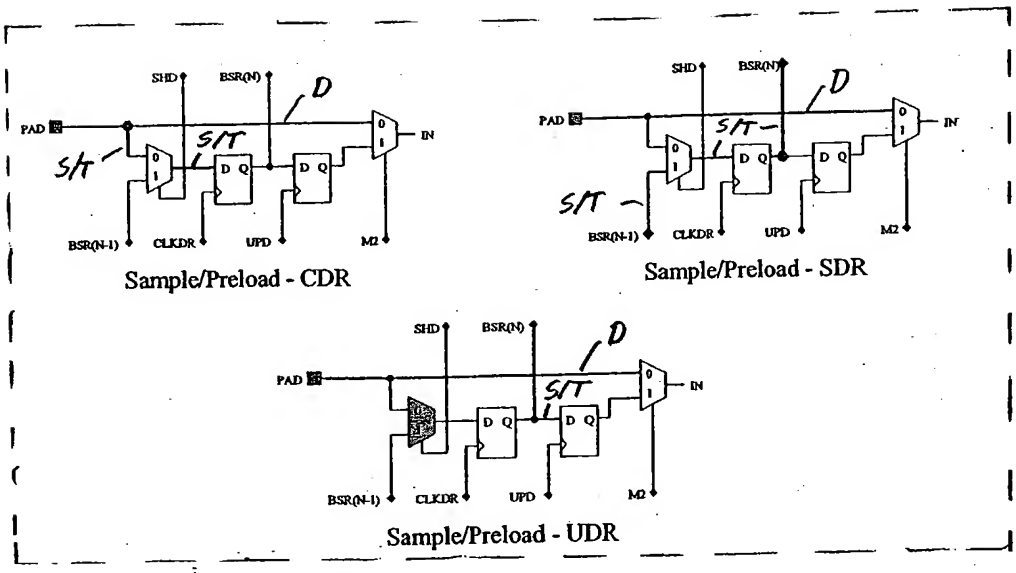


Fig. 12 – Sample/Preload BSC Operation

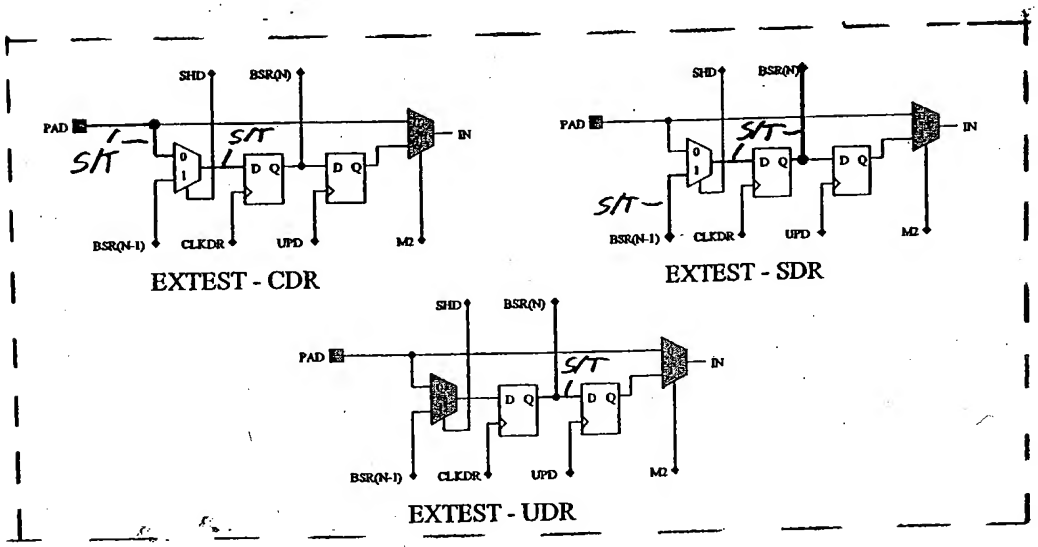


Fig. 13 – EXTEST BSC Operation

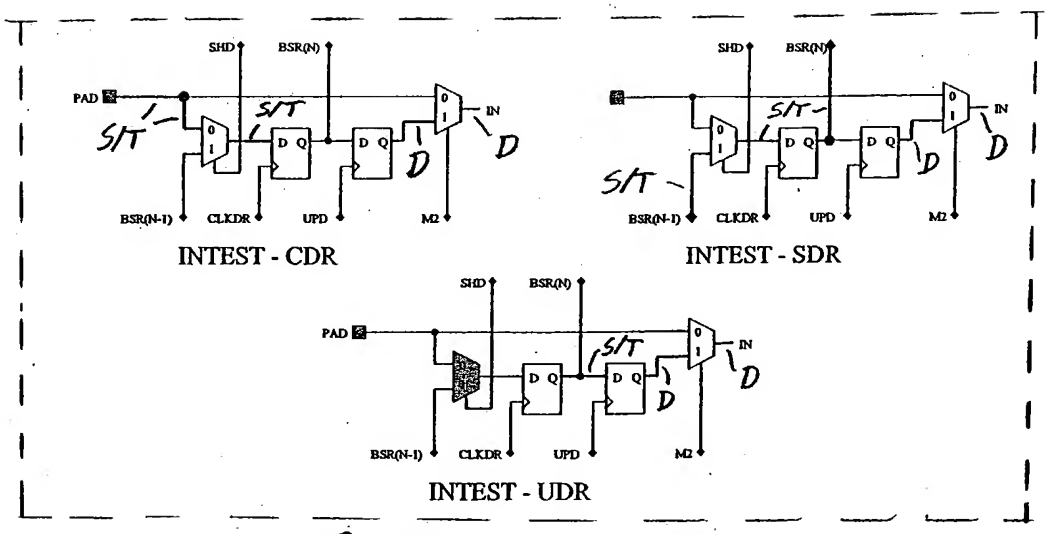
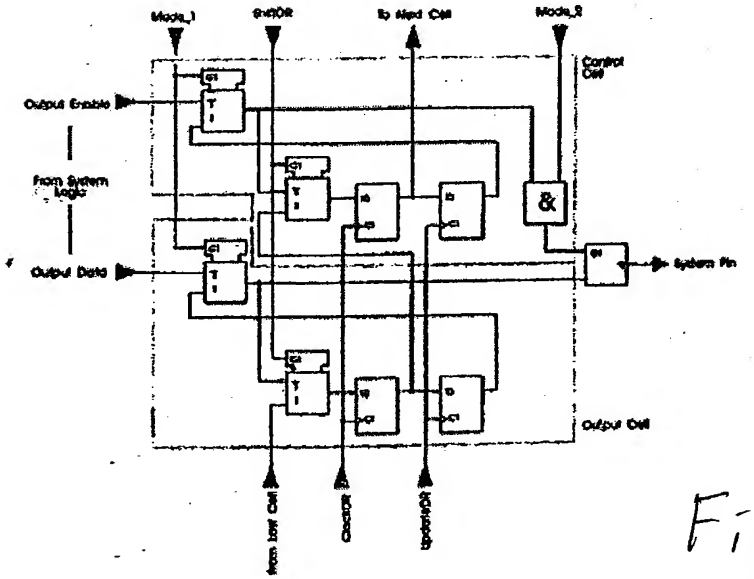


Fig. 14 – INTEST BSC Operation



1500

Fig. 15

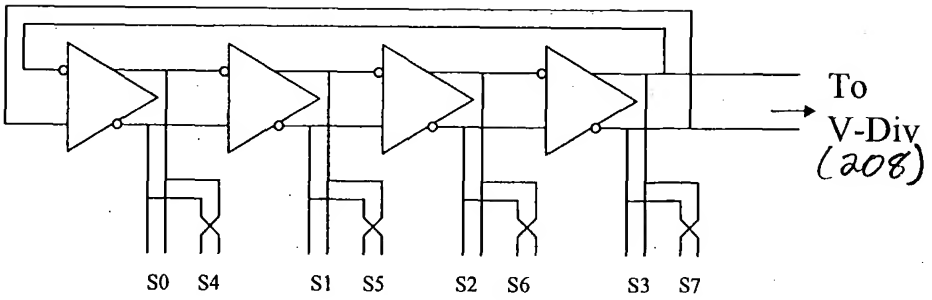

To
V-Div
(208)
S0
S4
S1
S5
S2
S6
S3
S7

Fig. 16

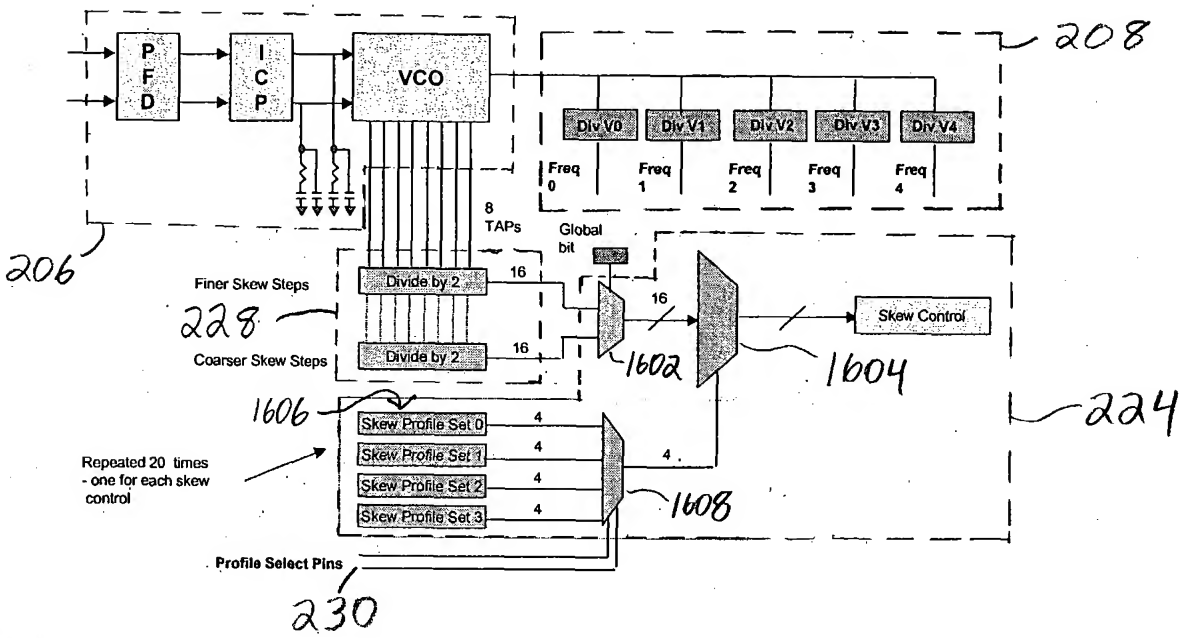

208
P
F
D
I
C
P
VCO
Div V0
Div V1
Div V2
Div V3
Div V4
Freq 0
Freq 1
Freq 2
Freq 3
Freq 4
206
8 TAPs
Global bit
Finer Skew Steps
228
Coarser Skew Steps
Divide by 2
Divide by 2
16
16
16
1602
1604
Skew Control
224
1606
Skew Profile Set 0
Skew Profile Set 1
Skew Profile Set 2
Skew Profile Set 3
4
4
4
4
4
1608
Repeated 20 times
- one for each skew
control
Profile Select Pins
230

Fig. 17

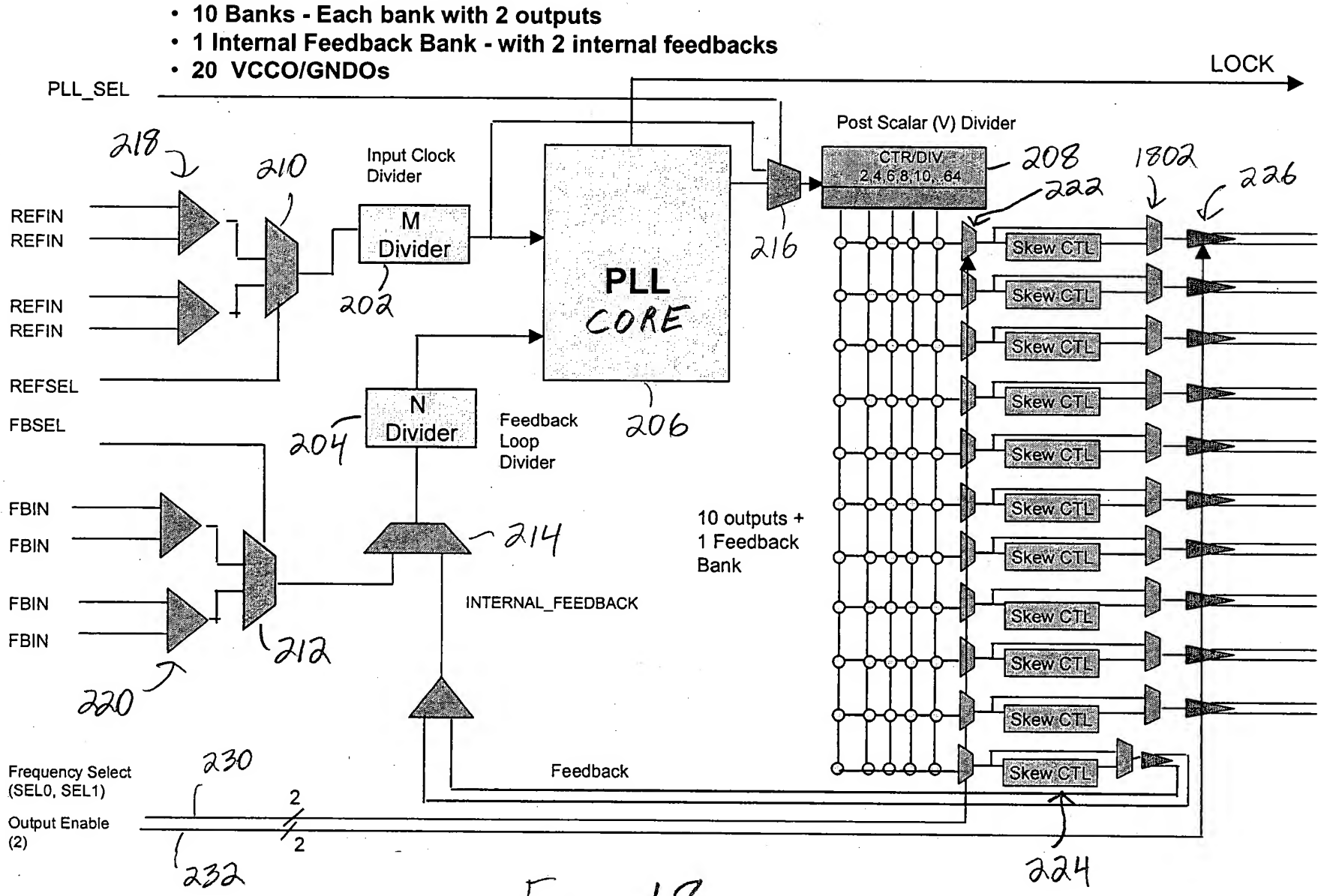

• 10 Banks - Each bank with 2 outputs
• 1 Internal Feedback Bank - with 2 internal feedbacks
• 20 VCCO/GNDOs
PLL_SEL
LOCK
Post Scalar (V) Divider
CTR/DIV
2,4,6,8,10...64
208
1802
226
222
218
210
Input Clock
Divider
M
Divider
202
REFIN
REFIN
REFIN
REFIN
REFSEL
FBSEL
PLL
CORE
206
216
N
Divider
204
Feedback
Loop
Divider
214
FBIN
FBIN
FBIN
FBIN
212
220
INTERNAL_FEEDBACK
10 outputs +
1 Feedback
Bank
Skew CTL
Skew CTL
Skew CTL
Skew CTL
Skew CTL
Skew CTL
Skew CTL
Skew CTL
Skew CTL
Skew CTL
Feedback
Frequency Select
(SEL0, SEL1)
230
2
Output Enable
(2)
2
232
224

Fig. 18

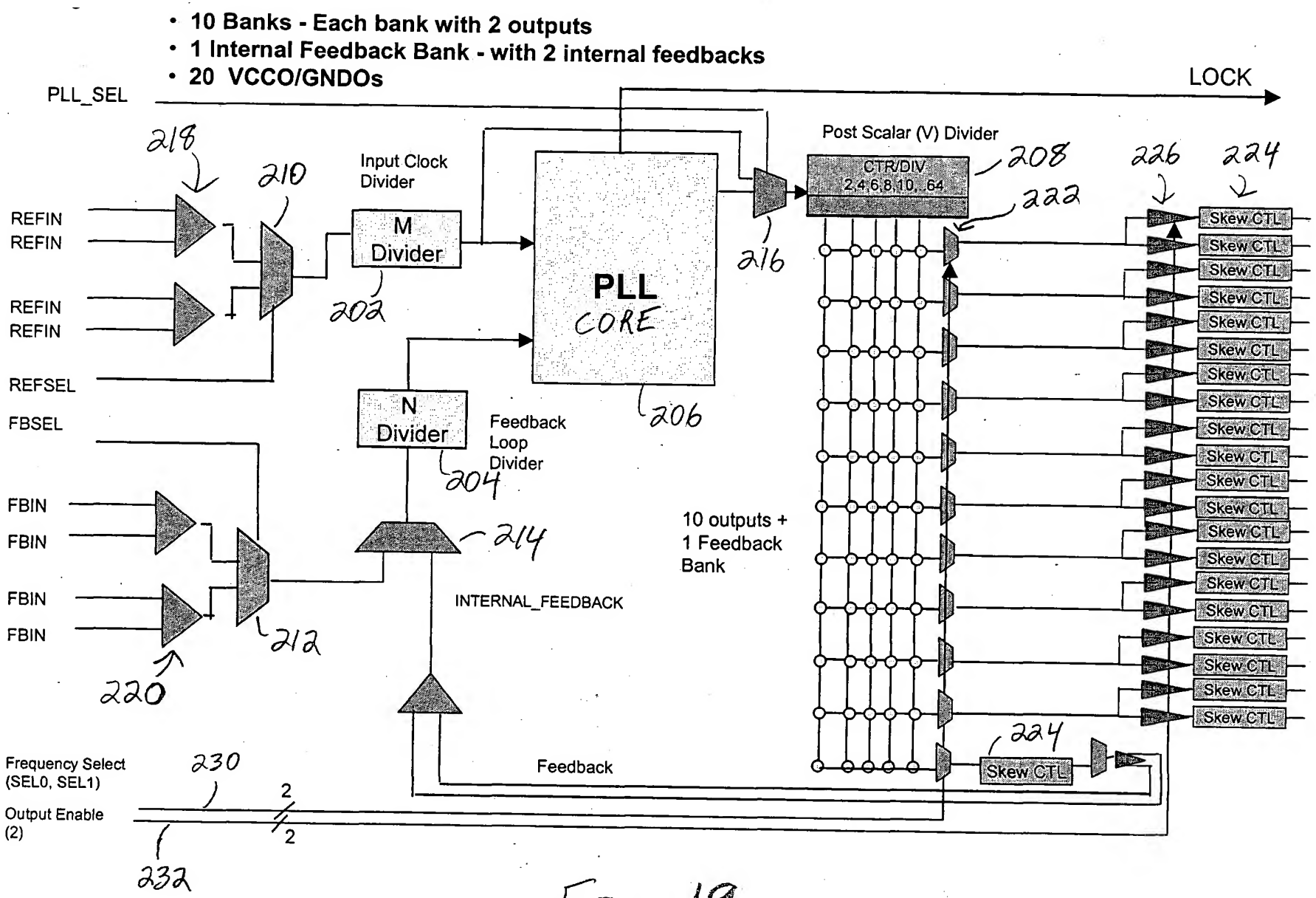

• 10 Banks - Each bank with 2 outputs
• 1 Internal Feedback Bank - with 2 internal feedbacks
• 20 VCCO/GNDOs
PLL_SEL
LOCK
218
210
Input Clock Divider
REFIN
REFIN
REFIN
REFIN
REFSEL
M Divider
202
PLL CORE
206
216
Post Scalar (V) Divider
CTR/DIV 2,4,6,8,10...64
208
222
226
224
Skew CTL
N Divider
204
Feedback Loop Divider
FBSEL
FBIN
FBIN
FBIN
FBIN
214
INTERNAL_FEEDBACK
212
220
10 outputs + 1 Feedback Bank
Frequency Select (SEL0, SEL1)
230
Output Enable (2)
2
2
232
Feedback

Fig. 19